SPI FLASH

2.5V/3.3V

4M-BIT

64KB SECTORS, DUAL AND QUAD SPI

1. DESCRIPTION

The CW20Q40GL (4M-Bit) Serial Flash memories provide a storage solution for systems with limited space, pins and power. The 20Q series offers flexibility and high performance. They are ideal for code backup, executing code directly from Dual/Quad SPI and storing voice, text, data, serial number and pattern. The device operates on a single 2.5V to 3.3V power supply with low current consumption.

The CW20Q40GL arrays are organized into 2048 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time. The CW20Q40GL have 8 erasable 64KB sectors, 1 erasable 512KB block.

The CW20Q40GL support the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O. The SPI I/O signals are I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported data rates of 26MB/s (104MHz x 2) for Dual I/O and 52MB/s (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O instructions. The Continuous Read Mode allows for efficient memory access with reduced 8-clocks of instruction-overhead.

A Hold pin, Write Protect pin and programmable write protect provides further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 64-bit Unique Serial Number.

2. FEATURES

- **Memory Architecture**
  - 4M-bit/512K-byte (524288)
  - 256-bytes per programmable page
  - 64KB sectors, 512KB block
- **SPI with Single / Dual / Quad IO**
  - Standard SPI: CLK, /CS, DI, DO, /WP, /HOLD
  - Dual SPI: CLK, /CS, IO0, IO1, /WP, /HOLD
  - Quad SPI: CLK, /CS, IO0, IO1, IO2, IO3
- **Data Transfer up to 416M-bits/second**
  - Clock operation to 104MHz
  - Dual – 208Mb/s
  - Quad – 416Mb/s
  - Auto-increment Read capability
- **Efficient Continuous Read mode**
  - Low instruction overhead
  - Continuous Read
- **Software and Hardware Write Protect**
  - Write Protect all or partial memory
  - Enable/Disable protection with /WP pin
- **Access Information**
  - Uniform Sector/Block Erase
  - Program one to 256bytes <10ms
  - More than 10K erase/write cycles
  - More than 10-year data retention
- **Low Power, Wide Temperature Range**
  - Single 2.5 to 3.3V supply
  - 2mA active current, 100uA power-down
  - -40°C to +85°C operating range
- **Space Efficient Packaging**
  - 8-pin SOIC

3. Pin Description

3.1 Pin Configuration

Pin function reference for CW20Q40GL

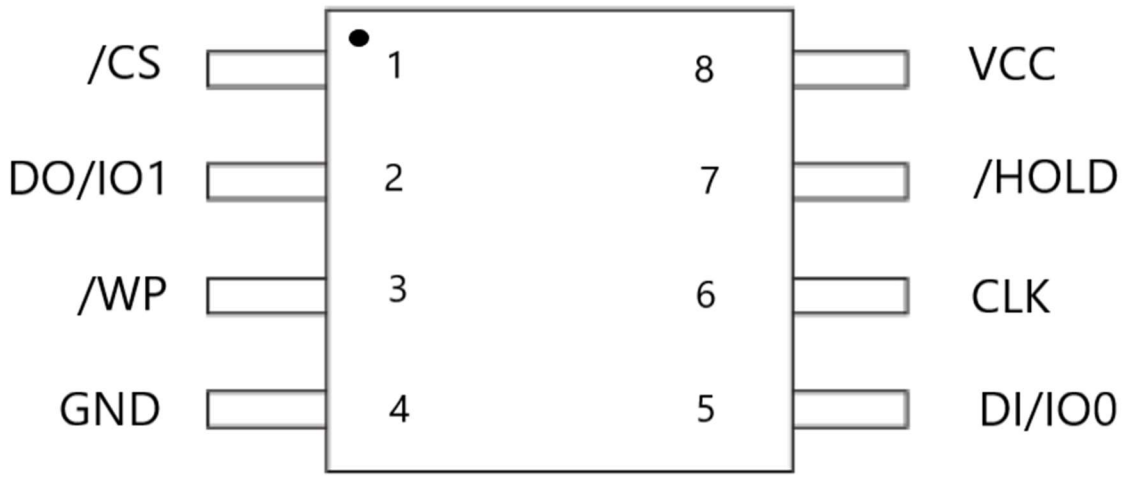

Figure 1. CW20Q40GL Pin assignment, 8-pin SOP

3.2 Pin Definition

PWR: Power or ground pin

A I: Analog input pin

A O: Analog output pin

A I/O: Analog input/output pin

I: Digital input pin

O: Digital output pin

I/O: Digital input/output pin

CW20Q40GL pin function description

Pin No.	Symbol	Pin Type	Description
8	VCC	PWR	IO power 3.3V Power input.
7	/HOLD	I/O	Hold input / Data in/out -bit3
6	CLK	I	Serial clock input
5	DI	I/O	Data input / Data in/out -bit0
4	GND	PWR	Ground
3	/WP	I/O	Write Protect input / Data in/out -bit2
2	DO	I/O	Data output / Data in/out -bit1
1	/CS	I	Chip select input

3.3 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables chip operation. When /CS is high, the device is disabled and the Data IO pins are at high impedance mode. When deselected, the devices power consumption will be at standby mode unless an internal erase, program or write status register operation is in progress.

3.4 Serial Data Input, Output and IOs

The CW20Q40GL support standard SPI, Dual SPI 2bits and Quad SPI 4bits operation. Standard SPI instructions use the DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock pin. Standard SPI also uses the DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

Quad SPI instructions require the Quad Enable bit (QE) in Status Register to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

3.5 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the data and Status Register from being written. The /WP pin is active low. When the QE bit of Status Register is set for Quad I/O, the /WP pin function is not available since this pin is used for IO2.

3.6 Hold (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is de-asserted, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When /HOLD is asserted to high, device operation can resume.

3.7 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the data synchronization operations.